08/931,133

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```
     (FILE 'USPAT' ENTERED AT 16:39:47 ON 07 MAY 1998)
L1             0 S (MEMORY TIM### (W) CONTROL###) AND ((WRIT### DATA FILE#)
 (P
L2             0 S (MEMORY TIM### (W) CONTROL###) AND ((WRIT### DATA FILE#)
 AN
L3        170200 S MEMORY (P) (TIM### OR CONTROL####)
L4             0 S WRIT### DATA FILE# AND (CACHE MEMORY (P) HOST SYSTEM)
L5         49279 S WRIT### (5W) (DATA OR DATA FILE# OR INFORMATION)
L6            38 S HOST SYSTEM (P) CACHE MEMORY
L7            15 S L5 (P) L6
L8           299 S FLASH EEPROM MEMORY
L9            14 S L7 (P) L3
L10       107874 S 395/CLAS OR 371/CLAS OR 365/CLAS OR 360/CLAS OR 364/CLAS
L11            9 S L10 AND L9
                  SAVE CHUNG/L ALL
```

=> d l9 cit 1-14

1. 5,732,241, Mar. 24, 1998, Random access cache memory controller and system; Alfred K. Chan, 711/131 [IMAGE AVAILABLE]

2. 5,682,500, Oct. 28, 1997, System and method for determining sequential cache data access in progress; Natan Vishlitzky, et al., 711/113 [IMAGE AVAILABLE]

3. 5,649,156, Jul. 15, 1997, Cache management system utilizing a cache data replacer responsive to cache stress threshold value and the period of time a data element remains in cache; Natan Vishlitzky, et al., 711/136, 113 [IMAGE AVAILABLE]

4. 5,596,736, Jan. 21, 1997, Data transfers to a backing store of a dynamically mapped data storage system in which data has nonsequential logical addresses; Randy G. Kerns, 711/4; 364/245, DIG.1; 711/100, 170, 171, 172, 202, 203 [IMAGE AVAILABLE]

5. 5,537,568, Jul. 16, 1996, System for dynamically controlling cache manager maintaining cache index and controlling sequential data access; Moshe Yanai, et al., 711/118; 364/243.41, 246.12, 251, DIG.1; 711/130, 136, 170 [IMAGE AVAILABLE]

6. 5,535,372, Jul. 9, 1996, Method and apparatus for efficient updating of CKD data stored on fixed block architecture devices; Michael T. Benhase, et al., 395/500; 360/48; 711/100 [IMAGE AVAILABLE]

7. 5,522,032, May 28, 1996, Raid level 5 with free blocks parity cache; Peter A. Franaszek, et al., 395/182.04; 371/51.1 [IMAGE AVAILABLE]

8. 5,513,336, Apr. 30, 1996, System and method for determining when and what position in cache memory to store data elements utilizing least and last accessed data replacement method; Natan Vishlitzky, et al., 711/136; 364/243.41, 246.12, DIG.1; 711/113 [IMAGE AVAILABLE]

9. 5,488,709, Jan. 30, 1996, Cache including decoupling register circuits; Alfred K. Chan, 711/118, 131, 143, 149 [IMAGE AVAILABLE]

10. 5,381,539, Jan 10, 1995, System and method for dynamically controlling cache management; Moshe Yanai, et al., 711/133; 364/243.41, 246.12, DIG.1; 711/129 [IMAGE AVAILABLE]

11. 5,257,352, Oct. 26, 1993, Input/output control method and system; Akira Yamamoto, et al., 711/136, 113, 114 [IMAGE AVAILABLE]

12. 5,148,537, Sep. 15, 1992, Method and apparatus for effecting an intra-cache data transfer; Jay S. Belsan, 711/131; 364/230.6, 239, 239.1, 239.7, 243, 243.4, 243.41, 244, 244.8, 246, 246.2, 260, 260.2, DIG.1; 711/130, 165 [IMAGE AVAILABLE]

13. 4,920,478, Apr. 24, 1990, Cache system used in a magnetic disk controller adopting an LRU system; Akihiko Furuya, et al., 711/136; 364/238.3, 238.4, 243, 243.4, 259.2, DIG.1; 711/113 [IMAGE AVAILABLE]

14. 4,835,686, May 30, 1989, Cache system adopting an LRU system, and magnetic disk controller incorporating it; Akihiko Furuya, et al., 711/136; 364/232.8, 236.2, 238.4, 242.3, 243, 243.4, 243.41, 244, 244.3, 246, 246.1, 246.11, 246.12, 248.1, 254.3, 259, 259.2, DIG.1; 711/113 [IMAGE AVAILABLE]

9. 4,835,686, May 30[redacted]989, Cache system adopting an [redacted] system, and magnetic disk controller incorporating it; Akihiko Furuya, et al., 711/136; **364/232.8, 236.2, 238.4, 242.3, 243, 243.4, 243.41, 244, 244.3, 246, 246.1, 246.11, 246.12, 248.1, 254.3, 259, 259.2, DIG.1**; 711/113 [IMAGE AVAILABLE]

=> d l11 kwic 5

US PAT NO: 5,513,336 [IMAGE AVAILABLE] L11: 5 of 9
US-CL-CURRENT: ~~711/136;~~ **364/243.41, 246.12, DIG.1**; 711/113

SUMMARY:

BSUM(24)

The presently described cache management system also includes a method for monitoring and **controlling** the contents of **cache memory** coupled to at least one data storage device. The method includes establishing and maintaining a cache directory including at least an indication of which data elements are currently in the **cache memory** and which data elements must be **written** to longer term **data** storage along with a **time** indication with each indexed data element indicating what **time** the data element was placed in cache. User selectable criteria are established including a sequential data access threshold, for providing a predetermined minimum number of data elements stored in the **cache memory** indicating the occurrence of a sequential data access in progress by at least one **host system** if the sequential data elements occur with a predetermined period of **time**.

SUMMARY:

BSUM(26)

After **writing** the **data** element to the longer term data storage device and determining the period of **time** the data element resided in the first section of the **cache memory**, the cache management system of the present invention next determines the average elapsed period of **time** that one or more data elements have spent in a second **cache memory** section, awaiting final removal from the **cache memory** entirely. A second section of **cache memory** is allocated to those data elements which have been **written** to a longer term **data** storage device but which, due to the short amount of **time** they have spent in cache, are maintained in **cache memory** in the event that a **host system** may call upon the data again.

DETDESC:

DETD(8)

The second section 17 of **cache memory** 12 is used to provide **memory** storage locations for those data elements which have been **written** to a longer term **data** storage device but which, due to the amount of **time** that they have resided in **cache memory**, the present cache management system has determined should remain in cache to ensure that the data element is available in the event that a **host system** wishes to again access the data element.

DETDESC:

DETD(13)

In . . . a data processing system such as a data storage system incorporating the present cache manager does not wait for device **controllers** 20a-20n to read or **write data** directly to or from the appropriate data storage device(s) and the host but rather, data to be **written** to or read from the **data** storage device(s) to the host is routed through and stored in **cache memory** 12. The present cache manager is directed to both data storage device read requests by a **host system**, and write requests from the host to the longer term data storage device. In the preferred embodiment, **cache memory** 12 includes high speed semiconductor **memory** whose data is rapidly accessible to both the device **controllers** 20 and the host adapters 24.

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     (FILE 'USPAT' ENTERED AT 16:39:47 ON 07 MAY 1998)
L1             0 S (MEMORY TIM### (W) CONTROL###) AND ((WRIT### DATA FILE#)
 (P
L2             0 S (MEMORY TIM### (W) CONTROL###) AND ((WRIT### DATA FILE#)
 AN
L3        170200 S MEMORY (P) (TIM### OR CONTROL####)
L4             0 S WRIT### DATA FILE# AND (CACHE MEMORY (P) HOST SYSTEM)
L5         49279 S WRIT### (5W) (DATA OR DATA FILE# OR INFORMATION)
L6            38 S HOST SYSTEM (P) CACHE MEMORY
L7            15 S L5 (P) L6
L8           299 S FLASH EEPROM MEMORY
L9            14 S L7 (P) L3
L10       107874 S 395/CLAS OR 371/CLAS OR 365/CLAS OR 360/CLAS OR 364/CLAS
L11            9 S L10 AND L9
                  SAVE CHUNG/L ALL
```

=> d l11 cit 1-9

1. 5,596,736, Jan. 21, 1997, Data transfers to a backing store of a dynamically mapped data storage system in which data has nonsequential logical addresses; Randy G. Kerns, 711/4; **364/245, DIG.1;** 711/100, 170, 171, 172, 202, 203 [IMAGE AVAILABLE]

2. 5,537,568, Jul. 16, 1996, System for dynamically controlling cache manager maintaining cache index and controlling sequential data access; Moshe Yanai, et al., 711/118; **364/243.41, 246.12, 251, DIG.1;** 711/130, 136, 170 [IMAGE AVAILABLE]

3. 5,535,372, Jul. 9, 1996, Method and apparatus for efficient updating of CKD data stored on fixed block architecture devices; Michael T. Benhase, et al., **395/500; 360/48;** 711/100 [IMAGE AVAILABLE]

4. 5,522,032, May 28, 1996, Raid level 5 with free blocks parity cache; Peter A. Franaszek, et al., **395/182.04; 371/51.1** [IMAGE AVAILABLE]

5. 5,513,336, Apr. 30, 1996, System and method for determining when and what ~~position~~ in cache memory to store data elements utilizing least and last accessed data replacement method; Natan Vishlitzky, et al., 711/136; **364/243.41, 246.12, DIG.1;** 711/113 [IMAGE AVAILABLE]

6. 5,381,539, Jan. 10, 1995, System and method for dynamically controlling cache management; Moshe Yanai, et al., 711/133; **364/243.41, 246.12, DIG.1;** 711/129 [IMAGE AVAILABLE]

7. 5,148,537, Sep. 15, 1992, Method and apparatus for effecting an intra-cache data transfer; Jay S. Belsan, 711/131; **364/230.6, 239, 239.1, 239.7, 243, 243.4, 243.41, 244, 244.8, 246, 246.2, 260, 260.2, DIG.1;** 711/130, 165 [IMAGE AVAILABLE]

8. 4,920,478, Apr. 24, 1990, Cache system used in a magnetic disk controller adopting an LRU system; Akihiko Furuya, et al., 711/136; **364/238.3, 238.4, 243, 243.4, 259.2, DIG.1;** 711/113 [IMAGE AVAILABLE]

access is in progress for a given process and provides an indication of the same. The system and method allocate a micro-cache memory to any process performing a sequential data access. In response to the indication of a sequential data access in progress and to a user selectable maximum number of data elements to be prefetched, a data retrieval requestor requests retrieval of up to the selected maximum number of data elements from a data storage device. A user selectable number of sequential data elements determines when previously used micro-cache memory locations will be overwritten. A method of dynamically monitoring and adjusting cache management parameters is also presented.

6. 5,535,372, Jul. 9, 1996, Method and apparatus for efficient updating of CKD data stored on fixed block architecture devices; Michael T. Benhase, et al., 395/500; 360/48; 711/100 [IMAGE AVAILABLE]

US PAT NO: 5,535,372 [IMAGE AVAILABLE] L9: 6 of 14

ABSTRACT:
A method and apparatus for updating CKD data stored on fixed block media, and more particularly to creating Track Format Descriptors which are data structures loaded into electronic memory to enable fast writing of data without loading an entire CKD emulated track of data into memory. A control unit is provided with logic to provide Track Format Descriptors which describe the format of the track without the need for the data content of the track to be resident in cache, or electronic memory. An emulated CKD volume corresponds to a volume of data stored on a multi-disk device. Each track on a volume is represented by a Track Format Descriptor. The Track Format Descriptor forms a representation of the format according to the following general procedure. If the format is a predefined format, in other words one that is already known by the control unit then a track form descriptor is formed to represent the format. If the format is easily discernible, it is said to be "well behaved". "Well behaved" formats are ones in which either each record has the same field length, there is no key field, or record numbers start at one and increment by one. A Track Format Descriptor is formed by predicting the format of these so called "well behaved" formats. If the format is not "well behaved" and the format has not been predefined, then the entire data track must be loaded into cache memory, before a fast write operation is performed. The Track Format Descriptor serves as an index to other information data structures which are loaded into memory when required by logic in the control unit.

7. 5,522,032, May 28, 1996, Raid level 5 with free blocks parity cache; Peter A. Franaszek, et al., 395/182.04; 371/51.1 [IMAGE AVAILABLE]

US PAT NO: 5,522,032 [IMAGE AVAILABLE] L9: 7 of 14

ABSTRACT:
A system for writing data to a disk array includes a cache memory coupled to the disk array for storing data indicative of locations on the disk array and parity blocks associated with parity groups including the locations. Each of the parity blocks includes an identifier indicative of locations within a particular parity group which are protected by the parity data. Write logic reads the identifier from the parity block, and based thereon, determines whether a disk location is not protected by the parity data. The write logic also writes to the location and updates the parity data and the identifier associated with the parity block to include the location of the data block to indicate that the location is protected.

8. 5,513,336, Apr. 30, 1996, System and method for determining when and what position in cache memory to store data elements utilizing least and last accessed data replacement method; Natan Vishlitzky, et al., 711/136; 364/243.41, 246.12, DIG.1; 711/113 [IMAGE AVAILABLE]

US PAT NO: 5,513,336 [IMAGE AVAILABLE] L9: 8 of 14

ABSTRACT:
A cache management system and method monitors and controls the contents of cache memory. Cache memory is organized into at least a first section for storing data waiting to be written to a longer term data storage device, and a second section for storing data elements which have been written to the longer term data storage device. A time indication provider provides a time indication signal to a cache indexer, for maintaining a cache index representing data elements which are stored in cache as well as an indication that a data element must be written to a longer term data storage device. A cache manager is responsible for placing data elements into and removing data elements from the cache memory. The cache manager determimes the amount of time that the data element has been stored in cache as well as the average period of time that elapses between a data element being inserted in cache and being removed from cache. Based on a comparison of the average period of time a data element spends in cache, and the amount of time a data element spends in cache, and the amount of time that the element has been stored in cache, the cache manager determines whether to place the data element in the top of the cache, to allow the data element to remain in cache a longer period of time, or at the bottom of the cache which will cause the data element to be removed from cache more quickly.

9. 5,488,709, Jan. 30, 1996, Cache including decoupling register circuits; Alfred K. Chan, 711/118, 131, 143, 149 [IMAGE AVAILABLE]

US PAT NO: 5,488,709 [IMAGE AVAILABLE] L9: 9 of 14

ABSTRACT:
A memory cache apparatus compatible with a wide variety of bus transfer types including non-burst and burst transfers. The memory cache apparatus includes a random access memory, a host port, and a system port. The memory cache apparatus further includes an input register connected to the host port for selectively writing data to the random access memory and an output register connected to the system port for receiving data from the random access memory and selectively furnishing the data to the host port or the system port. In one embodiment, the input register is a memory write register, and the output register includes a read hold register and a write back register. A cache memory system decouples a main memory subsystem from a host data bus so as to accommodate parallel cache-hit and system memory transfer operations for increased system speed and to hide system memory write-back cycles from a microprocessor. Differences in the speed of the local and system buses are accommodated, and an easy migration path from non-burst mode microprocessor based systems to burst mode microprocessor based systems is provided. Various memory organizations are accommodated including direct-mapped or one-way set associative, two-way set associative, and four-way set associative.

10. 5,381,539, Jan. 10, 1995, System and method for dynamically controlling cache management; Moshe Yanai, et al., 711/133; 364/243.41, 246.12, DIG.1; 711/129 [IMAGE AVAILABLE]

US PAT NO: 5,381,539 [IMAGE AVAILABLE] L9: 10 of 14

ABSTRACT:
A cache management system and method monitors and controls the contents of cache memory coupled to at least one host and at least one data storage device. A cache indexer maintains a current index of data elements which are stored in cache memory. A sequential data access indicator, responsive to the cache index and to a user selectable sequential data access threshold, determines that a sequential data access is in progress for a given process and provides an indication of the same. The system and method allocate a micro-cache memory to any process performing a sequential data access. In response to the

indication of a sequential data access in progress and to a user selectable maximum number of data elements to be prefetched, a data retrieval requestor requests retrieval of up to the selected maximum number of data elements from a data storage device. A user selectable number of sequential data elements determines when previously used micro-cache memory locations will be overwritten. A method of dynamically monitoring and adjusting cache management parameters is also presented.

11. 5,257,352, Oct. 26, 1993, Input/output control method and system; Akira Yamamoto, et al., 711/136, 113, 114 [IMAGE AVAILABLE]

US PAT NO: 5,257,352 [IMAGE AVAILABLE] L9: 11 of 14

ABSTRACT:
An input/output control apparatus connected to a plurality of input/output units such as disc systems and an input/output control method. A cache memory is divided into a plurality of storage areas for data management. Data stored in the disc systems are stored in the storage areas. In response to an output request from a HOST system to the disc systems, data outputted from the latter are stored in the storage areas of the cache memory. The data stored in the storage areas and outputted therefrom in response to the output request are transferred to the disc systems. The storage areas storing the data requested and not yet stored in the disc systems are grouped correspondingly to the disc systems where the output data are to be stored. The resulting group is managed as a first attribute group. Write-after processing for every disc units can be executed in parallel efficiently without involving high processing overhead.

12. 5,148,537, Sep. 15, 1992, Method and apparatus for effecting an intra-cache data transfer; Jay S. Belsan, 711/131; 364/230.6, 239, 239.1, 239.7, 243, 243.4, 243.41, 244, 244.8, 246, 246.2, 260, 260.2, DIG.1; 711/130, 165 [IMAGE AVAILABLE]

US PAT NO: 5,148,537 [IMAGE AVAILABLE] L9: 12 of 14

ABSTRACT:
A method and apparatus for effecting a transfer of data between different areas of a memory. Memory reading circuitry and memory writing circuitry are both connected to loopback switching apparatus. The loopback switching apparatus is controllably operable to interconnect the read circuitry with the write circuitry. This permits the data read out of a first memory area to be extended to the write circuitry for entry into a second memory area.

13. 4,920,478, Apr. 24, 1990, Cache system used in a magnetic disk controller adopting an LRU system; Akihiko Furuya, et al., 711/136; 364/238.3, 238.4, 243, 243.4, 259.2, DIG.1; 711/113 [IMAGE AVAILABLE]

US PAT NO: 4,920,478 [IMAGE AVAILABLE] L9: 13 of 14

ABSTRACT:
A magnetic disk controller incorporating a cache memory which employs an LRU (Least Recently Used) scheme in a replacement algorithm of cache blocks and comprising a directory memory whose entries have LRU counter fields, a host system issuing a read/write command to which an arbitrary LRU settling value is appended, a directory search circuit, and a microprocessor. The directory search circuit searches the directory memory in response to the read/write command issued from the host system. The microprocessor stores the LRU setting value appended to the read/write command in the LRU counter field of the hit entry of the directory memory or of the entry corresponding to the repalacement target cache block, in response to the search result of the directory search circuit.

14. 4,835,686, May 30, 1989, Cache system adopting an LRU system, and magnetic disk controller incorporating it; Akihiko Fukuoya, et al., 711/136; 364/232.8, 236.2, 238.4, 242.3, 243, 243.4, 243.41, 244, 244.3, 246, 246.1, 246.11, 246.12, 248.1, 254.3, 259, 259.2, DIG.1; 711/113 [IMAGE AVAILABLE]

US PAT NO: 4,835,686 [IMAGE AVAILABLE] L9: 14 of 14

ABSTRACT:
A cache system employing an LRU (Least Recently Used) scheme in a replacement algorithm of cache blocks and comprising a directory memory whose entires have LRU counter fields, a host system issuing a read/write command to which an arbitrary LRU setting value is appended, a directory search circuit, and a microprocessor. The directory search circuit searches the directory memory in response to the read/write command issued from the host system. The microprocessor stores the LRU setting value appended to the read/write command in the LRU counter field of the hit entry of the directory memory or of the entry corresponding to the replacement target cache block, in response to the search result of the directory search circuit.

S PAT NO: 5,649,156 [IMAGE AVAILABLE] L9: 3 of 14

SUMMARY:

BSUM(24)

The presently described cache management system also includes a method for monitoring and **controlling** the contents of **cache memory** coupled to at least one data storage device. The method includes establishing and maintaining a cache directory including at least an indication of which data elements are currently in the **cache memory** and which data elements must be **written** to longer term **data** storage along with a **time** indication with each indexed data element indicating what **time** the data element was placed in cache. User selectable criteria are established including a sequential data access threshold, for providing a predetermined minimum number of data elements stored in the **cache memory** indicating the occurrence of a sequential data access in progress by at least one **host system** if the sequential data elements occur with a predetermined period of **time**.

SUMMARY:

BSUM(26)

After **writing** the **data** element to the longer term data storage device and determining the period of **time** the data element resided in the first section of the **cache memory**, the cache management system of the present invention next determines the average elapsed period of **time** that a data element spends in a second **cache memory** section, awaiting final removal from the **cache memory** entirely. A second section of **cache memory** is allocated to those data elements which have been **written** to a longer term **data** storage device but which, due to the short amount of **time** they have spent in cache, are maintained in **cache memory** in the event that a **host system** may call upon the data again.

DETDESC:

DETD(7)

The second section 17 of **cache memory** 12 is used to provide **memory** storage locations for those data elements which have been **written** to a longer term **data** storage device but which, due to the amount of **time** that they have resided in **cache memory**, the present cache management system has determined should remain in cache to ensure that the data element is available in the event that a **host system** wishes to again access the data element.

DETDESC:

DETD(12)

In . . . a data processing system such as a data storage system incorporating the present cache manager does not wait for device **controllers** 20a-20n to read or **write data** directly to or from the appropriate data storage device(s) and the host but rather, data to be **written** to or read from the **data** storage device(s) to the host is routed through and stored in **cache memory** 12. The present

cache manager is directed to both data storage devices for read requests by a **host system**, and writes requests from the host to the longer term data storage device. In the preferred embodiment, **cache memory** 12 includes high speed semiconductor **memory** whose data is rapidly accessible to both the device **controllers** 20 and the host adapters 24.

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     (FILE 'USPAT' ENTERED AT 16:39:47 ON 07 MAY 1998)
L1             0 S (MEMORY TIM### (W) CONTROL###) AND ((WRIT### DATA FILE#)
 (P
L2             0 S (MEMORY TIM### (W) CONTROL###) AND ((WRIT### DATA FILE#)
 AN
L3        170200 S MEMORY (P) (TIM### OR CONTROL####)
L4             0 S WRIT### DATA FILE# AND (CACHE MEMORY (P) HOST SYSTEM)
L5         49279 S WRIT### (5W) (DATA OR DATA FILE# OR INFORMATION)
L6            38 S HOST SYSTEM (P) CACHE MEMORY
L7            15 S L5 (P) L6
L8           299 S FLASH EEPROM MEMORY
L9            14 S L7 (P) L3
L10       107874 S 395/CLAS OR 371/CLAS OR 365/CLAS OR 360/CLAS OR 364/CLAS
L11            9 S L10 AND L9
                  SAVE CHUNG/L ALL
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=> d l9 cit, ab 1-14

1. 5,732,241, Mar. 24, 1998, Random access cache memory controller and system; Alfred K. Chan, 711/131 [IMAGE AVAILABLE]

US PAT NO: 5,732,241 [IMAGE AVAILABLE] L9: 1 of 14

ABSTRACT:
A memory cache apparatus compatible with a wide variety of bus transfer types including non-burst and burst transfers. In burst mode, a "demand word first" wrapped around quad fetch order is supported. The cache memory system decouples the main memory subsystem from the host data bus so as to accommodate parallel cache-hit and system memory transfer operations for increased system speed and to hide system memory write-back cycles from the microprocessor. Differences in the speed of the local and system buses are accommodated, and an easy migration path from non-burst mode microprocessor based systems to burst mode microprocessor based systems is provided. Various memory organizations are accommodated including direct-mapped or one-way set associative, two-way set associative, and four-way set associative.

2. 5,682,500, Oct. 28, 1997, System and method for determining sequential cache data access in progress; Natan Vishlitzky, et al., 711/113 [IMAGE AVAILABLE]

US PAT NO: 5,682,500 [IMAGE AVAILABLE] L9: 2 of 14

ABSTRACT:
A dynamic cache management system and method monitors and controls the contents of cache memory coupled to at least one host and at least one data storage device. A cache indexer maintains a current index of data elements which are stored in cache memory along with a time indication which relates to each data elements use in the cache. A sequential data access indicator, responsive to the cache index, to the time indication associated with each data element and to a user selectable data access threshold, determines that a sequential data access is in progress for a given process and provides an indication of the same. The system and method allocate a micro-cache memory to any process performing a sequential data access. In response to the indication of a sequential

data access in progress and to a user selectable maximum number of data elements to be prefetched, a data retrieval requestor requests retrieval of up to the selected maximum number of data elements from a data storage device. A user selectable number of sequential data elements determines when previously used micro-cache memory locations will be overwritten.

3. 5,649,156, Jul. 15, 1997, Cache management system utilizing a cache data ~~replacer~~ responsive to cache stress threshold value and the period of time a data element remains in cache; Natan Vishlitzky, et al., 711/136, 113 [IMAGE AVAILABLE]

US PAT NO: 5,649,156 [IMAGE AVAILABLE] L9: 3 of 14

ABSTRACT:
A cache management system and method monitors and controls the contents of cache memory coupled to at least one longer term data storage device. Cache memory is organized into at least first and second sections, the first section for storing data waiting to be written to a longer term data storage device and the second section for storing data elements which have been written to the longer term data storage device. The cache management system and method monitors data elements awaiting writing to the longer term data storage device. Once the elements have been actually written to the longer term data storage device, the cache management system and method utilizes an indication of the amount of time the data element was in cache as well as an indication of the number of times the data element was accessed, in order to determine how long to maintain the data record in the short term cache

4. 5,596,736, Jan. 21, 1997, Data transfers to a backing store of a dynamically mapped data storage system in which data has nonsequential logical addresses; Randy G. Kerns, 711/4; 364/245, DIG.1; 711/100, 170, 171, 172, 202, 203 [IMAGE AVAILABLE]

US PAT NO: 5,596,736 [IMAGE AVAILABLE] L9: 4 of 14

ABSTRACT:
A destaging method for a mapped data storage system is provided for writing data to a backing store. Data having non-sequential logical addresses are grouped together. The data includes data segments. A maximal difference in size between two data segments is less than a predetermined value. A constructed data segment includes a particular data item when the particular data item has a logical address between logical addresses of two other data items when they are part of this same constructed data segment. After being grouped together, such data is destaged from a cache memory to the backing store. Data from a group is transferred to an unallocated storage area of the backing store nearest to the physical position of the data transfer head responsible for the transfer. Each such transfer is continuous while reducing seek and/or latency delays and without regard to the nonsequential logical addresses of the data being transferred.

5. 5,537,568, Jul. 16, 1996, System for dynamically controlling cache manager maintaining cache index and controlling sequential data access; Moshe Yanai, et al., 711/118; 364/243.41, 246.12, 251, DIG.1; 711/130, 136, 170 [IMAGE AVAILABLE]

US PAT NO: 5,537,568 [IMAGE AVAILABLE] L9: 5 of 14

ABSTRACT:
A cache management system and method monitors and controls the contents of cache memory coupled to at least one host and at least one data storage device. A cache indexer maintains a current index of data elements which are stored in cache memory. A sequential data access indicator, responsive to the cache index and to a user selectable sequential data access threshold, determines that a sequential data

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US PAT NO: 5,257,352 [IMAGE AVAILABLE] L9: 11 of 14

SUMMARY:

BSUM(3)

As one of the cache managing or **controlling** techniques for a disc **controller** equipped with a cache known heretofore, there may be mentioned a system disclosed in JP-A-55-117780 according to which slots, i.e. data storage units for the **cache memory** are managed with the aid of a single LRU (Least Recently Used) chain. Correspondence relation is established between the individual slots and tracks of a disc unit which is under the **control** of the disc **controller**. Upon reception of data to be written in the disc unit (hereinafter also referred to as the **write data**) from a **HOST system**, the disc **controller writes** the **data** not only in the cache but also in the disc unit. Accordingly, coincidence is always found between the content of. . .

SUMMARY:

BSUM(19)

In a **controller** connected to input/output units, cache memories are put in groups by every input/output unit to which the **write**-pending **data** stored in the **cache memory** is to be written. In response to an input/output request issued from a **HOST system**, data is inputted/outputted to/from the cache memories. Subsequently, the data placed in the cache memories are transferred to the input/output. . .

CLAIMS:

CLMS(25)

25. An input/output **control** apparatus according to at least one input/output unit and cooperating with a **host system**, said **control** apparatus comprising:

a **cache memory** logically divided into a plurality of storage areas;

a directory having a plurality of storage area management information corresponding to said **cache memory** storage areas;

means for loading data from said input units into said **cache memory** storage areas;

means for **writing data** from said **cache memory** storage areas into said output units in response to an output request from said **host system**; and

means for correspondingly grouping those of said **cache memory** storage areas in which said requested output data are stored but have not yet been written to said output units to those of said output units to which said requested output data is to be written, said grouped **cache memory** storage areas comprising a writing attribute group.

=> d his

(FILE 'USPAT' ENTERED AT 15:22:46 ON 07 MAY 1998)
L1 7163 S CACHE MEMORY OR TEMPORAR? MEMORY OR REDUNDANT MEMORY OR SP
L2 982 S FLASH EEPROM MEMORY OR FLASH EEPROM
L3 (1620081)S TIM###
L4 3308 S L1 (P) L3
L5 12 S L4 (P) L2
L6 356 S TAG MEMORY
L7 6 S L5 (P) L6
SAVE PHUNG/L ALL
L8 128430 S 395/CLAS OR 364/CLAS OR 365/CLAS OR 360/CLAS OR 371/CLAS OR
L9 6 S L7 AND L8

=> d l9 cit 1-6

1. 5,719,808, Feb. 17, 1998, Flash EEPROM system; Eliyahou Harari, et al., **365/185.33, 185.22, 185.29** [IMAGE AVAILABLE]

2. 5,671,229, Sep. 23, 1997, Flash eeprom system with defect handling; Eliyahou Harari, et al., **371/10.2; 365/200; 395/182.01, 182.03** [IMAGE AVAILABLE]

3. 5,602,987, Feb. 11, 1997, Flash EEprom system; Eliyahou Harari, et al., **395/182.06; 365/200, 210;** 711/100 [IMAGE AVAILABLE]

4. 5,535,328, Jul. 9, 1996, Non-volatile memory system card with flash erasable sectors of EEprom cells including a mechanism for substituting defective cells; Eliyahou Harari, et al., **395/182.05; 364/268.5, DIG.1; 365/218; 395/182.06, 833;** 711/115 [IMAGE AVAILABLE]

5. 5,418,752, May 23, 1995, Flash EEPROM system with erase sector select; Eliyahou Harari, et al., **365/218, 185.09, 185.11, 185.22, 185.29** [IMAGE AVAILABLE]

6. 5,297,148, Mar. 22, 1994, Flash eeprom system; Eliyahou Harari, et al., **371/10.2; 365/185.09, 185.33, 200; 371/10.3; 395/182.05** [IMAGE AVAILABLE]